

## WHAT IS CLAIMED IS:

1           1.    For use in an operational circuit having a high impedance  
2 node, a pre-charge circuit capable of pre-charging said high-  
3 impedance node to a target voltage when a pre-charge signal driving  
4 said pre-charge circuit is enabled, said pre-charge circuit  
5 comprising:

6                a charge voltage circuit capable of charging an internal  
7 common node of said pre-charge circuit to said target voltage when  
8 said pre-charge signal is enabled;

9                a transmission gate switch capable of coupling said  
10 internal node to said high-impedance node when said pre-charge  
11 signal is enabled, said transmission gate switch comprising a first  
12 N-channel transistor having a drain coupled to said high-impedance  
13 node, a gate coupled to a Logic 1 when said pre-charge signal is  
14 enabled, and a source coupled to said internal common node; and

15               a gate-biasing circuit driven by said pre-charge signal,  
16 wherein said gate-biasing circuit is off when said pre-charge  
17 signal is enabled and generates a negative Vgs bias on said first  
18 N-channel transistor when said pre-charge signal is disabled to  
19 thereby reduce leakage current in said first N-channel transistor.

1           2.    The pre-charge circuit as set forth in Claim 1 wherein  
2   said transmission gate switch further comprises a first P-channel  
3   transistor having a drain coupled to said high-impedance node, a  
4   gate coupled to a Logic 0 when said pre-charge signal is enabled,  
5   and a source coupled to said internal common node.

1           3.    The pre-charge circuit as set forth in Claim 2 wherein  
2   said gate-biasing circuit generates a positive Vgs bias on said  
3   first P-channel transistor when said pre-charge signal is disabled  
4   to thereby reduce leakage current in said first P-channel  
5   transistor.

1           4.    The pre-charge circuit as set forth in Claim 3 wherein  
2   said gate of said first N-channel transistor is coupled to a Logic  
3   0 when said pre-charge signal is disabled and said gate-biasing  
4   circuit holds said internal common node at a voltage higher than  
5   Logic 0 to thereby generate said negative Vgs bias on said first N-  
6   channel transistor when said pre-charge signal is disabled.

1           5.    The pre-charge circuit as set forth in Claim 4 wherein  
2   said gate of said first P-channel transistor is coupled to a Logic  
3   1 when said pre-charge signal is disabled and said gate-biasing  
4   circuit holds said internal common node at a voltage less than  
5   Logic 1 to thereby generate said positive Vgs bias on said first P-  
6   channel transistor when said pre-charge signal is disabled.

1           6.    The pre-charge circuit as set forth in Claim 5 wherein  
2   said charge voltage circuit comprises a first diode-connected  
3   transistor and a second diode-connected transistor, wherein said  
4   first and second diode-connected transistors are connected as  
5   diodes in series between a VDD power supply rail and a ground rail  
6   when said pre-charge signal is enabled and wherein said internal  
7   common node is a connection node between said first and second  
8   diode-connected transistors.

1           7.    The pre-charge circuit as set forth in Claim 6 wherein  
2   said target voltage is determined by an impedance of said first  
3   diode-connected transistor and an impedance of said second diode-  
4   connected transistor when said pre-charge signal is enabled.

1           8.    The pre-charge circuit as set forth in Claim 7 wherein  
2   said impedance of said first diode-connected transistor and said  
3   impedance of said second diode-connected transistor are equal when  
4   said pre-charge signal is enabled and said target voltage is equal  
5   to  $VDD/2$ .

1           9.    The pre-charge circuit as set forth in Claim 7 wherein  
2   said first and second diode-connected transistors are off when said  
3   pre-charge signal is disabled.

1           10.   The pre-charge circuit as set forth in Claim 9 wherein  
2   said gate-biasing circuit holds said internal common node at said  
3   target voltage when said pre-charge circuit is disabled.

1        11. A signal generator comprising a phase-locked loop (PLL)  
2 circuit capable of generating an output reference signal having a  
3 desired frequency, said PLL circuit comprising:  
4            a voltage-controlled oscillator;  
5            a charge pump and loop filter circuit for generating a  
6 control voltage capable of controlling said voltage controlled  
7 oscillator; and  
8            a pre-charge circuit capable of pre-charging said high-  
9 impedance node of said charge pump and loop filter to a target  
10 voltage when a pre-charge signal driving said pre-charge circuit is  
11 enabled, said pre-charge circuit comprising:  
12            a charge voltage circuit capable of charging an  
13 internal common node of said pre-charge circuit to said target  
14 voltage when said pre-charge signal is enabled;  
15            a transmission gate switch capable of coupling said  
16 internal node to said high-impedance node when said pre-charge  
17 signal is enabled, said transmission gate switch comprising a  
18 first N-channel transistor having a drain coupled to said  
19 high-impedance node, a gate coupled to a Logic 1 when said  
20 pre-charge signal is enabled, and a source coupled to said  
21 internal common node; and

22                   a gate-biasing circuit driven by said pre-charge  
23           signal, wherein said gate-biasing circuit is off when said  
24           pre-charge signal is enabled and generates a negative Vgs bias  
25           on said first N-channel transistor when said pre-charge signal  
26           is disabled to thereby reduce leakage current in said first N-  
27           channel transistor.

1           12. The signal generator as set forth in Claim 11 wherein  
2           said transmission gate switch further comprises a first P-channel  
3           transistor having a drain coupled to said high-impedance node, a  
4           gate coupled to a Logic 0 when said pre-charge signal is enabled,  
5           and a source coupled to said internal common node.

1           13. The signal generator as set forth in Claim 12 wherein  
2           said gate-biasing circuit generates a positive Vgs bias on said  
3           first P-channel transistor when said pre-charge signal is disabled  
4           to thereby reduce leakage current in said first P-channel  
5           transistor.

1        14. The signal generator as set forth in Claim 13 wherein  
2        said gate of said first N-channel transistor is coupled to a Logic  
3        0 when said pre-charge signal is disabled and said gate-biasing  
4        circuit holds said internal common node at a voltage higher than  
5        Logic 0 to thereby generate said negative Vgs bias on said first N-  
6        channel transistor when said pre-charge signal is disabled.

1        15. The signal generator as set forth in Claim 14 wherein  
2        said gate of said first P-channel transistor is coupled to a Logic  
3        1 when said pre-charge signal is disabled and said gate-biasing  
4        circuit holds said internal common node at a voltage less than  
5        Logic 1 to thereby generate said positive Vgs bias on said first P-  
6        channel transistor when said pre-charge signal is disabled.

1        16. The signal generator as set forth in Claim 15 wherein  
2        said charge voltage circuit comprises a first diode-connected  
3        transistor and a second diode-connected transistor, wherein said  
4        first and second diode-connected transistors are connected as  
5        diodes in series between a VDD power supply rail and a ground rail  
6        when said pre-charge signal is enabled and wherein said internal  
7        common node is a connection node between said first and second  
8        diode-connected transistors.

1        17. The signal generator as set forth in Claim 16 wherein  
2 said target voltage is determined by an impedance of said first  
3 diode-connected transistor and an impedance of said second diode-  
4 connected transistor when said pre-charge signal is enabled.

1        18. The signal generator as set forth in Claim 17 wherein  
2 said impedance of said first diode-connected transistor and said  
3 impedance of said second diode-connected transistor are equal when  
4 said pre-charge signal is enabled and said target voltage is equal  
5 to  $VDD/2$ .

1        19. The signal generator as set forth in Claim 17 wherein  
2 said first and second diode-connected transistors are off when said  
3 pre-charge signal is disabled.

1        20. The signal generator as set forth in Claim 19 wherein  
2 said gate-biasing circuit holds said internal common node at said  
3 target voltage when said pre-charge circuit is disabled.